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PATENT
5500-97900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Chen, et al

Serial No. 10/655,390

Filed: September 4, 2003

For: Method and System for Architectural Power Estimation

§ Group Art Unit: 2825
§ Examiner: Unknown
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§ Atty. Dkt. No. 5500-97900
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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below:

B. Noël Kivlin
Registered Representative

5-21-04 _____
Date Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3.

☒ A copy of each reference listed on the Form PTO-1449 is enclosed.
☐ The references listed on the Form PTO-1449 were previously cited in application serial no. _____ to which the captioned application is seeking priority under 35 U.S.C. §120; therefore, a copy of each reference is not enclosed.
☐ The captioned application was filed after June 30, 2003; therefore, a copy of each reference is not enclosed.

1. This Information Disclosure Statement is submitted:

a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☒ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure

Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 50-1505/5500-97900.

Respectfully submitted,

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Date: 5-21-04

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5500-97900 APPLICANT: Chen, et al FILING DATE: September 4, 2003	SERIAL NO. 10/655,390 GROUP: 2825

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE APPROPRIAT

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATIO YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A1	"Wattch: A Framework for Architectural-Level Power Analysis and Optimations", Brooks, et al, ISCA, 2000, Vancouver BC Canada, 1-58113-232-8/00/6.
	A2	"An Enhanced Access and Cycle Time Model for On-Chip Caches", Wilton, et al, Western Research Laboratory, Palo Alto, CA, July, 1994.
	A3	"Evaluation of Architecture-Level Power Estimation for CJMOS RISC Processors", Sato, et al, IEEE, 1995, 0 7803-3036-6/95.
	A4	"Power and Performance Simulator:ESP and its Application for 100MIPS/W Class RISC Design", Sato, et al, IEEE, 1994, 0-7803-1953-2/94
	A5	"A Technique to Determine Power-Efficient, High-Performance Superscalar Porcessors", Conte, et al, IEEE, 1995, 1060-3425/95
	A6	"Reducing Power in High-Performance Microprocessors", Tiwari, et al, ACM, San Diego, CA, 1998, 0-897-964-5/98/06.
	A7	"Instruction-Level Power Estimation for Embedded VLIW Cores", Sami, et al, ACM, San Diego, CA, 2000, 1 58114-268-9/00/5.
	A8	"Power Estimation of System-Level Buses for Microprocessor-Based Architectures: A Case Study", Fornaciari, et al, Proceeddings of the 1999 IEEE International Conference on Computer Design, October, 1999, Austin, TX.
	A9	"System-Level Power Optimization: Techniques and Tools", Benini, et al, ACM, San Diego, CA, 1999, 1-58113-133-X/99/0008.
	A10	"Architectural Level Hierarchical Power Estimation of Control Units", Chen, et al, IEEE, 1998, 0-7803-4980-6/98.
	A11	"Microprocessor Power Estimation Using Profile-Driven Program Synthesis", Hsieh, et al, IEEE, 1998, 0278-0070/98.

EXAMINER: DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.